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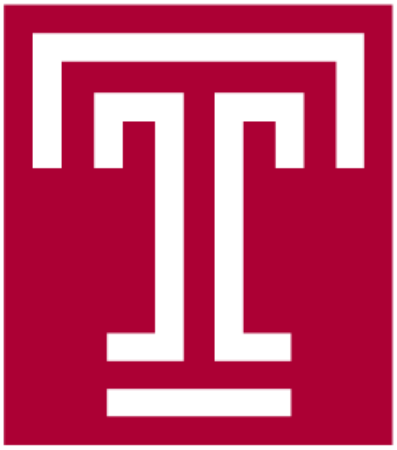

CIS 5603. ARTIFICIAL INTELLIGENCE

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Final Project: Virtual Teaching Assistant

INTRODUCTION

In undergraduate engineering, laboratories play an important role. The objectives of these laboratories are to reinforce the learning of new and developing subject matters, to enhance students' understanding of real world engineering problems, and to demonstrate how to approach those problems systematically [1][2] . Generally, students perform experiments in the laboratory for certain period in weekly basis under supervision of a teaching assistant. Such format of the laboratory is called closed laboratories. Closed laboratories have space and time constraints. As a result, students do not have much flexibility. Students, sometimes, need to work in groups because of the lack of sufficient number of equipment. Due to limited number of teaching assistants, not all students receive sufficient help on their labwork. There are office hours outside the laboratory time for students to meet the teaching assistant with their problems. Often times, students may not be able to utilize the opportunity because of their other classes. In summary, closed laboratories are not resource effective [3] .

The open laboratory model can mitigate scheduling and resource utilization related issues in the closed laboratory [4] [5] [6]. In an open laboratory, students can perform their experiments at any time. If necessary, they can repeat the experiments for better understanding. The open laboratory ensures maximum utilization of space and equipment. However, providing teaching assistants around the clock for open laboratories is challenging. Therefore, virtual teaching assistants are necessary.

In order to fill this gap, we developed a virtual teaching assistant for offering on-demand help to the students in an open laboratory. The system is called Virtual Open Laboratory Teaching Assistant (VOLTA). This web-based system is equipped with pre-laboratory instructions, topic

based explanations, equipment usage videos, assistance for performing circuit simulation and hardware experiment. Our approach of open laboratory provides a laboratory space, and facilitates performing the experiments outside the laboratory room as well. The previous open laboratory approaches put lower weight on teaching assistance aspect. They considered open laboratory approach would encourage students to solve their own problem, and eventually lead to increase self-confidence and learning [6]. VOLTA is designed to provide teaching assistance in virtual format reducing the dependency on human teaching assistants.

We assess the effectiveness of VOLTA using pre-test and post-test design methods on two groups of students: control and experimental groups. The objective of the study was to find out whether VOLTA can assist in students' learning like human teaching assistants.

ARCHITECTURE AND METHOD

Architecture of system

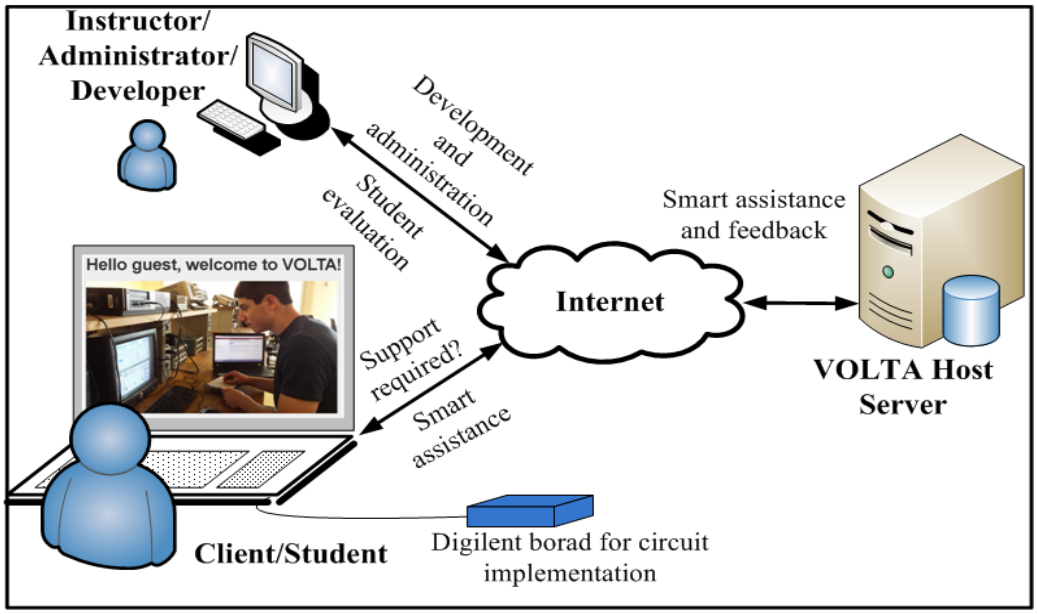

Fig 1

The architecture of the VOLTA is shown in Fig 1. As the Fig1 shows, the system including the

following components: instructor module, student module, help module, circuit comparator and circuit tracer module, implementation and user Interface. Here, we pay our attention to the circuit comparator, which is critical part of the system. In the following paragraphs, we use CC to indicate circuit comparator.

The Circuit Comparator (CC) is an intelligent circuit analysis module used in VOLTA to examine a student's simulation work, identify errors and provide explanations to improve answer. The CC provides users experiment instructions through VOLTA on how to build and simulate circuits based on lab manual.

In traditional circuit laboratory, if a student has a problem with his/her simulation result, he/she will call teaching assistant (TA), then TA will check the simulation circuit as follows:

a) Examine the student's circuit keeping in mind the objective of the experiment
b) Check if the circuit contains all required components
c) Check if the all components are connected properly as the lab manual illustrated

Circuit Comparator checks against with simulation circuit as follows:

1. CC matches elements between two netlist, in case of using unwanted source (incorrect amplitude voltage, incorrect frequency and so on), and additional elements.
2. Then CC checks topological connections according to node connections from netlists, so that CC checks if the two netlists build equivalent circuits.

The objective of CC is to verify if the student's simulation circuit is equivalent to the solution circuit. As long as a student builds a circuit on Multisim, he/she can generate a SPICE netlist file according to his/her circuit. The SPICE netlist contains component parameters, node connection with each component [7] . Then the student can upload his/her netlist file to VOLTA website, VOLTA website will return analysis result of his/her simulation.

CC was developed based on an intelligent circuit analysis module [8], it applied Graph Theory [3] and fundamental loop matrix computation algorithm [9]. CC is coded by Python, which runs faster.

The module of CC contains 1) VOLTA Circuit translator, 2) Component Check, 3) topology check, 4) result. The functional flow chart is shown in Fig.2.

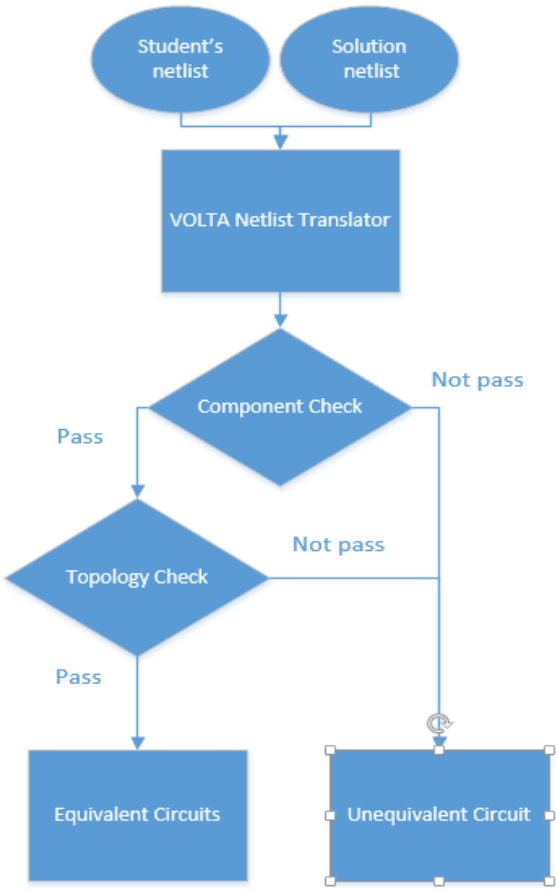

Fig2: Flow Chart of CC

Method

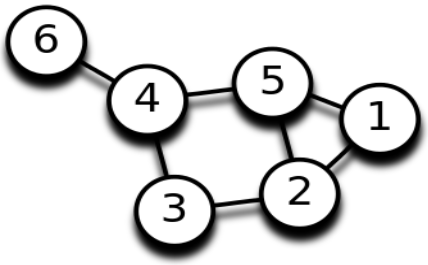

Fig3

Graph Theory: a graph (G): G = (V, E). A graph as shown in Fig3 is made up of vertices (V)

and edges (E). A graph may be undirected, meaning that there is no distinction between the two vertices associated with each edge, or its edges may be directed from one vertex to another.

A circuit is viewed as a graph [10] consisting of nodes and branches as shown in Fig 4. The nodes of the graph are connected by edges (circuit elements in our case). One of the basic laws in circuit theory Kirchoff's Voltage Law (KVL), states that the net voltage drop across various components in a circuit loop is zero. (A path that can be traced through a circuit starting from a node and ending at the same node without passing through a component more than once is called a circuit loop.) It is known that the corresponding branch currents and voltages should be identical in completely topologically equivalent circuits. From this, it follows that the loop currents and voltages should also be the same. If the fundamental loops (an independent circuit loop formed by a unique path through a chosen tree T along with each link of the cotree Tc of tree T) for both circuits under consideration are identified and the nature and orientation of components in corresponding fundamental loops are determined to be the same, then both circuits will have identical loop characteristics and thereby yield identical circuit solutions. In essence, the results of loop analysis for equivalent circuits should be the same.

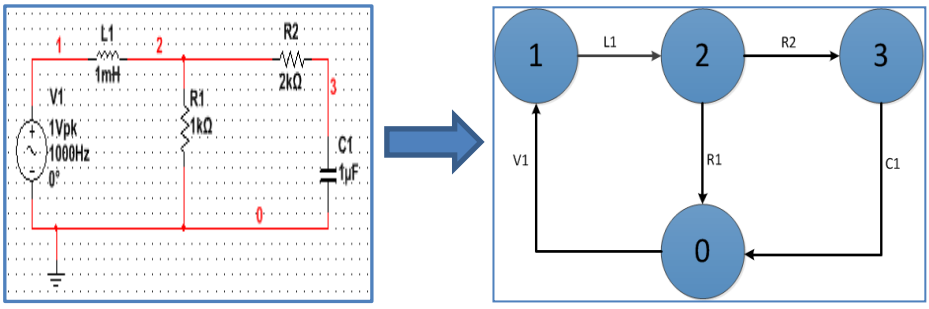

Fig4

In order to demonstrate the application of graph theory in circuit, we take some example to illustrate in subsequent prographs.

A student is required to build a RCL circuit with 1 volte pk-pk, 1 kHz voltage source, and 1mH inductor, 1kohm resistor, 1uF capacitor, then plot the capacitor voltage. He/she built the circuit on Multisim (Fig.5), and the TA built the solution circuit before and saved as solution circuit (Fig.6). It is clear that the two circuits are equivalent even the component order is different, the node label is not matching. So CC can shows that these two circuits are equivalent (Fig.7).

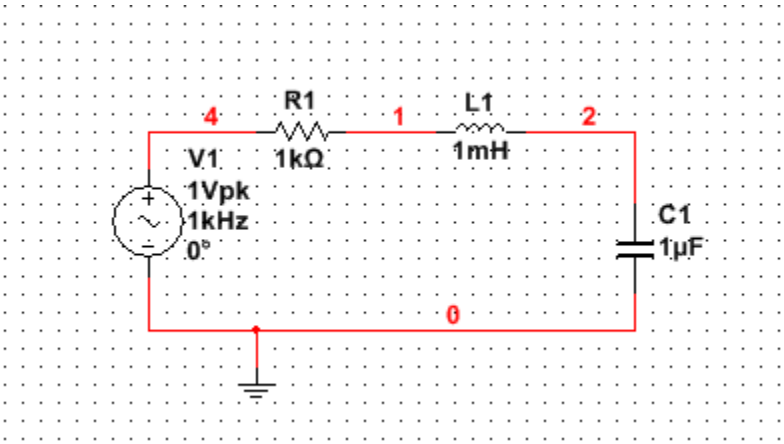

Fig 5 Student's Circuit

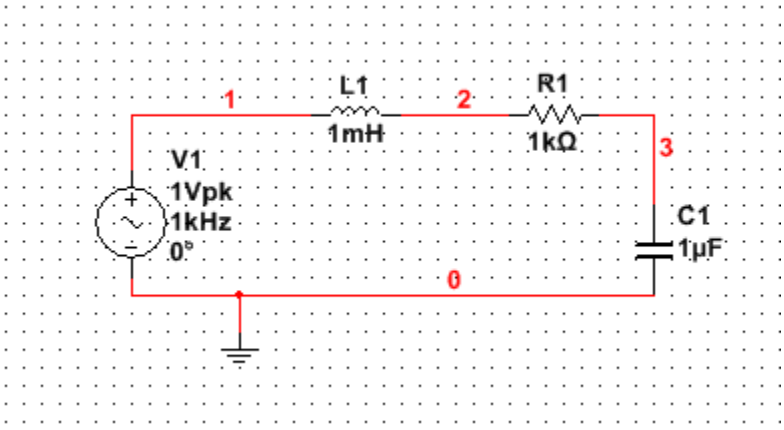

Fig 6 Solution Circuit

```
max number of node
number of element
[5, 4]
[[ 1. -1.  0.  0.]
 [ 0.  0.  1. -1.]
 [-1.  0.  0.  1.]
 [ 0.  0.  0.  0.]
 [ 0.  1. -1.  0.]]
{'C1': ['1e-06'], 'VAC1': ['1', '1000'], 'R1': ['1000'], 'L1': ['0.001']}
{'C1': [2, 0], 'VAC1': [0, 4], 'R1': [4, 1], 'L1': [1, 2]}
['VAC1', 'R1', 'L1', 'C1']
max number of node
number of element
[4, 4]
{'C1': ['1e-06'], 'VAC1': ['1', '1000'], 'R1': ['1000'], 'L1': ['0.001']}
{'C1': [3, 0], 'VAC1': [0, 1], 'R1': [2, 3], 'L1': [1, 2]}
[[ 1. -1.  0.  0.]
 [ 0.  1.  0. -1.]
 [ 0.  0. -1.  1.]
 [-1.  0.  1.  0.]]
['VAC1', 'L1', 'R1', 'C1']
equal
```

Figure 7 CC Result

Another student built a RCL circuit on Multisim with 1 volte pk-pk, 100 Hz voltage source, and 1mH inductor, 1kohm resistor, 1uF capacitor (Fig.8), but according to the lab manual, the solution circuit should consist of a sine wave AC voltage with 1 volte pk-pk, 100 Hz (Fig.9). So this student's circuit is not qualified, CC concluded that the two circuits are not equivalent (Fig.10).

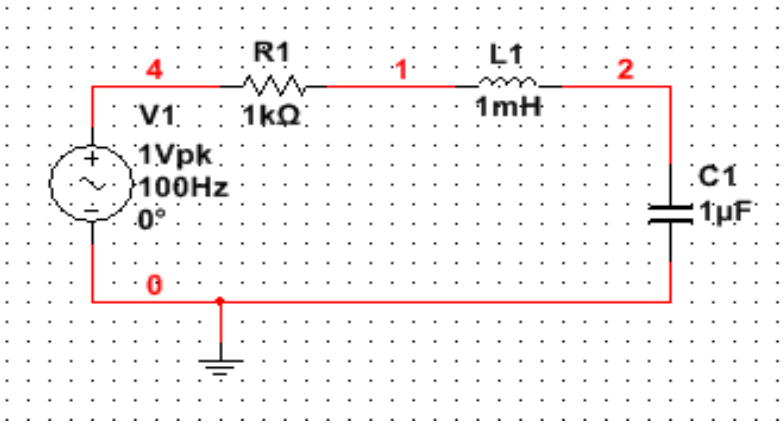

Fig 8 Student's circuit

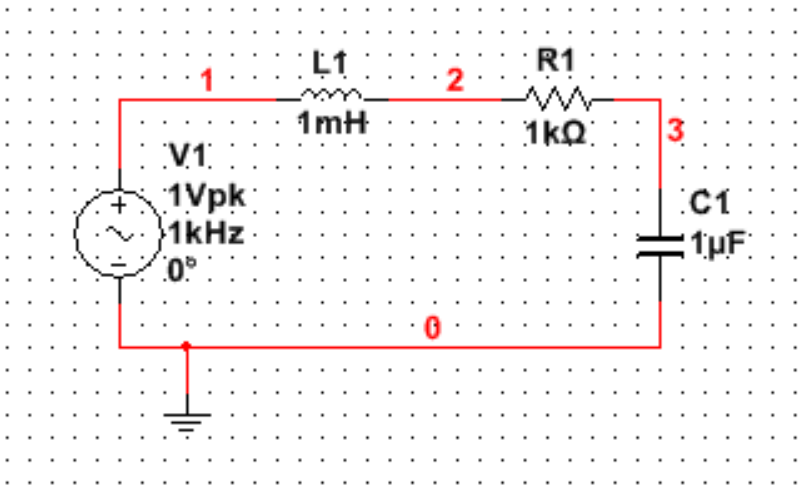

Fig 9 Solution circuit

```
zicong@zicong-OptiPlex-980: ~/Python comparator/new/test
.cir 22.cir
max number of node
number of element
[4, 4]
[[ 1. -1.  0.  0.]
 [ 0.  1.  0. -1.]
 [ 0.  0. -1.  1.]
 [-1.  0.  1.  0.]]
{'C1': ['1e-06'], 'VAC1': ['1', '1000'], 'R1': ['1000'], 'L1': ['0.001']}
{'C1': [3, 0], 'VAC1': [0, 1], 'R1': [2, 3], 'L1': [1, 2]}
['VAC1', 'L1', 'R1', 'C1']
max number of node
number of element
[5, 4]
{'C1': ['1e-06'], 'VAC1': ['1', '100'], 'R1': ['1000'], 'L1': ['0.001']}
{'C1': [2, 0], 'VAC1': [0, 4], 'R1': [4, 1], 'L1': [1, 2]}
[[ 1. -1.  0.  0.]
 [ 0.  0.  1. -1.]
 [-1.  0.  0.  1.]
 [ 0.  0.  0.  0.]
 [ 0.  1. -1.  0.]]
['VAC1', 'R1', 'L1', 'C1']
not equal
zicong@zicong-OptiPlex-980:~/Python comparator/new/test$
```

Fig 10 CC Result

EXPERIMENT RESULT

In addition, we test our system in mid-term examination.

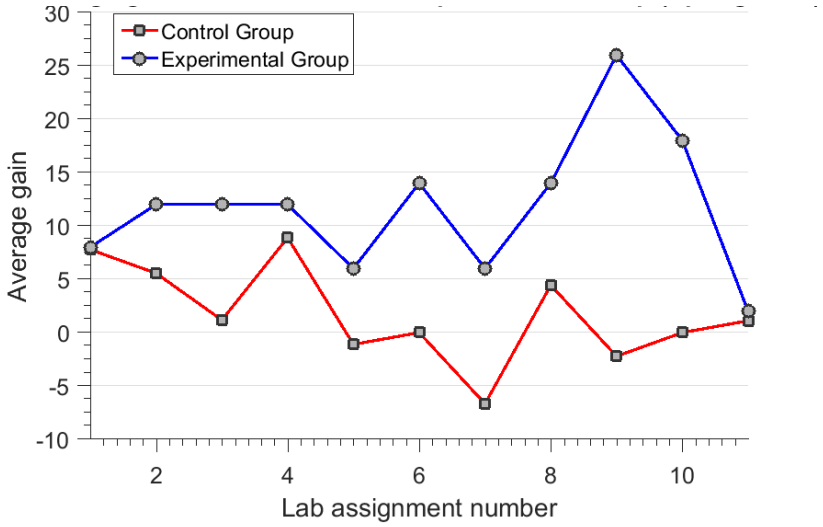

Fig11

There are two lab sections I teach in Spring 2016, traditional group (control group) and VOLTA group (experimental group). There are 11 students in control group and 11 students in experimental group. The traditional group students are taught by old-fashion way, the experimental group students are taught by virtual website. On each lab day, I give students pre-lab tests, and the end of lab, I give students post-lab tests. We define the gain, which is the difference between post-lab test (S2) and pre-lab test (S1).

Gain =S2-S1

We started our simulation checking function at lab6, according to Fig.11. We can see that the experiment group gains are normally higher than the traditional group. And since lab6, the experiment group performed better than before. We concluded the following reasons.

1. The Virtual website gave students accessibility to review lab theory, comparing to some students in traditional group never touch the paper-based lab manual again.

2. The simulation-checking program saved more time for TA and students, which helped them to learn from lab.
3. Students prefer YouTube videos and Google to learn rather than reading from book

The following tables are the student's score tables.

And we have a survey from virtual lab section, students gave normal and positive feedback to us. Of course, there are students think there are some things to be improved to virtual lab.

Table1: Traditional teaching lab

Lab Assignment no.	Pre-test		Post-test		Average gain
	Mean	Standard Deviation	Mean	Standard Deviation	
1	64.44	15.71	66.67	20.00	2.23
2	36.67	17.95	47.78	19.02	11.11
3	64.21	27.97	62.22	33.26	−1.99
4	51.76	13.82	48.24	22.81	−3.52
5	83.33	24.27	90.00	15.28	6.67
6	68.75	27.36	82.67	17.69	13.92
7	76.67	24.27	72.94	28.24	−3.73
8	76.00	23.32	82.67	17.69	6.67
9	71.11	20.25	76.47	12.34	5.36
10	52.50	26.34	65.00	27.84	12.50
11	68.57	23.56	70.59	21.82	2.02

Table2: Experiment Virtual teaching lab

Lab Assignment no.	Pre-test		Post-test		Average gain
	Mean	Standard Deviation	Mean	Standard Deviation	
1	58.89	22.58	71.11	23.31	12.22
2	47.14	17.90	40.01	18.52	−7.13
3	58.75	23.95	57.50	21.70	−1.25
4	68.57	26.95	65.00	24.66	−3.57
5	68.57	26.95	74.29	23.21	5.72
6	61.54	27.69	64.62	28.45	3.08
7	66.67	18.9	68.00	20.40	1.33
8	86.67	13.98	93.33	11.93	6.66
9	63.08	15.38	84.62	11.51	21.54
10	65.45	21.05	76.36	20.57	10.91
11	74.29	26.65	87.14	17.90	12.85

CONCLUSION

Through the project, we basically understand the fundamental of graph theory, how to apply it

into circuit analysis, and how to implement the algorithm using python. In addition, through this project, we know that artificial intelligence is not real intelligence but a version of intelligence which is designed by human. It is the outcome of human's intelligent effort.

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